REMARKS

Applicants appreciate the examination of the present application that is evidenced by the Official Action of September 21, 2005. In response to the Official Action, Applicants have corrected two typographical errors in the specification and have amended Claims 1, 16, 19, 23, 25 and 27. Claims 13-15, 17 and 30 have also been canceled. Applicants will now address each of the issues raised in the Official Action.

The Original Drawings Meet the Requirements of 37 CFR § 1.83

As described in the specification, the plurality of multi-frame data streams (e.g., 64 data streams) are provided as "data" signals to an input of a TSI switch. As understood by those skilled in the art, a multi-frame data stream is conventional and represents multiple bytes of serial data provided on a data bus. Examples of such data streams are illustrated by the prior art IDT datasheets provided on multiple information disclosure statements (see, e.g., FORM PTO-1449, filed May 16, 2001 and FORM PTO-1449, filed January 21, 2003). However, a "multi-frame data stream" is not a "feature" of the invention and does not need to be illustrated by the drawings. (See, e.g., 37 CFR 1.83(a)). Instead, a "multi-frame data stream" is merely a signal that the claimed switch is responsive to. This signal is described in detailed throughout the present application and the properties of such signals are well known to those skilled in the art.

Accordingly, Applicants respectfully submit that the originally filed drawings are more than adequate to meet the requirements of 37 CFR §1.83, because these requirements do not require the illustration of generic signals that provide no feature of the present invention.

The Claims Meet the Requirements of 35 USC § 112

1. Re: Claims 1-30.

Applicants respectfully disagree with the Examiner's assertion that the claimed subject matter is not adequately supported by the specification. With respect to the Examiner's assertion that "it is not clear to what reference the delay(s) and/or offset(s) are determined," Applicants submit that the calculation of delay and frame offsets are conventional and well known to those skilled in the art (see, e.g., FIG. 2, which illustrates how the frame delay bits relate to the clock period shift). In particular, the text at p. 7, line 15 - p. 8, line 15 of the specification explain how a "count" is maintained of how many clock pulses occur between receipt of the FOi signal and receipt of the frame evaluation (FE) signal for a respective data stream under evaluation. This number of clock pulses represents a degree to which the respective data stream is delayed relative to the FOi signal. As understood by those skilled in the art, this well known delay value represents a "frame offset" for a respective data stream.

2. Re: Claims 16-18.

Applicants also respectfully submit that the "summary of the invention" is part of the specification of the application, which means that terms used in the "summary of the invention" can be used to support claim recitations. Accordingly, Applicants submit that the Examiner's assertion that various claim recitations "are only stated in the summary" does not establish a lack of enablement with respect to the specification taken as a whole.

In any event, Applicants will now show that Claims 16-18 are adequately described in the specification. In Claim 16, first and second storage devices are recited. In dependent Claim 18, the first storage device is identified as a "register having M rows of storage units therein" and the second storage device is identified as retaining "an M-bit error code therein." In FIG. 3, a "register having M rows of storage units" is illustrated as the FOR Register **118** and the M-bit error code is illustrated as being stored within the Error Code Register **114**, where M=16.

Moreover, in FIG. 4, the binary representations of the "frame offsets" are illustrated by the 4-bit values stored within each segmented row of the FOR Register **118**. The 16-bits of data retained by the Error Code Register **114** in FIG. 4 identify the locations of unacceptable frame offsets (shown as "1111") in the FOR Register **118** of FIG. 4. This "identification" of the location of an unacceptable frame offset is provided by the "0" or "1" value of each of the 16-bits of code in the register **114**. If a bit is a "0", no unacceptable frame offsets are stored within the corresponding row of the FOR Register **118**. However, if a bit is a "1", then at least one unacceptable frame offset is stored within the corresponding row of the FOR Register **118**. These aspects of FIGS. 3-4 are more fully described in detail at page 10, lines 7-30 of the specification.

Claim 19 has been Amended to Address the Rejection under 35 USC § 112

As recited by Claim 19, a frame delay conversion circuit (block **106** in FIG. 3) is provided that converts the frame delays provided by the frame alignment counter (block **102** in FIG. 3) to frame offsets (see, e.g., offset bits <2:0> and DLE, which represent a 4-bit offset). The frame alignment counter **102** also generates an error signal, which is represented as carry signal (CARRY). This carry signal is provided to the error control circuit (block **112** in FIG. 3). If the error control circuit **112** receives an active carry signal (i.e., CARRY = 1), then it will generate an error override, which represents an unacceptable frame offset. This error override is provided to the write control logic **108**, which writes a "1111" value into the temporary register **110**. Thus, the temporary register **110** is configured to receive both acceptable frame offsets from the frame delay conversion circuit **106** and unacceptable frame offsets from the error control circuit **112**. These aspects of the invention are more fully described at p. 8, line 10 - p. 9, line 11; and p. 10, line 1 - p. 10, line 4; and p. 10, line 21 - p. 10, line 26 of the specification.

Based on this discussion and the amendments provided to Claim 19, Applicants respectfully submit that Claims 19-20 are in condition for allowance.

All Claims are Patentable Over the Cited Prior Art

Independent Claims 1, 16, 23 and 27 have been amended to highlight how the claimed switch retains data that identifies the locations of unacceptable frame offsets (or delays) within a register. As illustrated by FIGS. 3-4 of the application, the error code register **114** contains a 16-bit error code (Error Code <15:0> and each bit of this error code operates as a "pointer" that identifies a location within the FOR register **118**. If the error code bit for a particular row equals "1", then at least one unacceptable frame offset (or possibly an unacceptable frame delay) is present in the corresponding row of the FOR register **118**. Thus, the retained data (e.g., 16-bit error code) not only identifies whether an unacceptable frame offset is present, but it also identifies the location of the unacceptable frame offset. Applicants respectfully submit that this feature of the claimed invention is not disclosed or suggested by the cited prior art, including Applicants' admitted prior art (APA).

Respectfully submitted,

Grant J. Scott
Registration No. 36,925

Myers Bigel Sibley & Sajovec, P.A.
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401
Customer No. 20792

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 23, 2006..

Candi L. Riggs

#484575